What is claimed is:

1. A digital signal processor supporting a floating point, comprising:

a data register for storing data;

an inverter for receiving the data and negating when the data is a negative number;

a multiplexer for outputting an output value from the inverter and the data register in accordance with a predetermined rule;

an OR operator for performing a logical OR operation to an accumulated value and an output value from the multiplexer;

an accumulator for receiving and accumulating a result of the logical OR operation, and feedbacking the accumulated result to an input end of the OR operator; and

an exponent extractor for extracting an exponent from the accumulated result.

2. The digital signal processor supporting a floating point of claim 1, wherein the predetermined rule processes an ORC instruction and the result value of the inverter is outputted when the MSB (most significant bit) of the data is 1.

3. The digital signal processor supporting a floating point of claim 1, wherein the accumulator comprises:

a repeater having a loop structure for performing a repeated movement as much as the number of blocks of the data; and

a repeater counter for numbering the repeated movement.

4. The digital signal processor supporting a floating point of claim 3, wherein the accumulator stores a first number and last number of the block.

5. A digital signal processor supporting a floating point, comprising:

a program memory for storing a program with a predetermined instruction;

an instruction register for fetching and storing the instruction of the program;

a decoding and pipeline controller for decoding the instruction so as to control pile line needed for performing a correspondent instruction;

a data memory for storing data;

a program address generator for generating a program address to be currently performed and transmitting the program address to the program memory;

a data address generator generating a data address for inputting and outputting the data memory through a control of the decoding and pipeline controller;

an operating processor performing calculation, logic, multiplication for a data operation; and

a multiplier 270 for performing multiplication needed for the data operation.

6. The digital signal processor supporting a floating point of claim 5, wherein the operating processor comprises:

a data register for storing data;

an inverter for receiving the data and negating the data when the data is a negative number;

a multiplexer for outputting an output value from the inverter and the data register in accordance with a predetermined rule;

an OR operator for performing a logical OR operation to an accumulated value and an output value from the multiplexer;

an accumulator for receiving and accumulating a result of the logical OR operation, and feedbacking the accumulated result to an input end of the OR operator; and

an exponent extractor for extracting an exponent from the accumulated result.

7. The digital signal processor supporting a floating point of claim 6, wherein the operating processor comprises:

an adder and a divider for performing an operation except an ORC operation; and

a multiplexer for storing a result value of the OR operator to the accumulator when the currently performed instruction is the ORC operation, or storing the result value of the adder and the divider to the accumulator 150.

8. The digital signal processor supporting a floating point of claim 6, wherein the predetermined rule processes an ORC instruction and the result value of the inverter is outputted when the MSB (most significant bit) of the data is 1.

9. The digital signal processor supporting a floating point of claim 6, wherein the accumulator comprises:

a repeater having a loop structure for performing a repeated movement as much as the number of blocks of the data; and

a repeater counter for numbering the repeated movement.

10. The digital signal processor supporting a floating point of claim 6, wherein the accumulator stores a first number and last number of the block.